

**FIG 1**

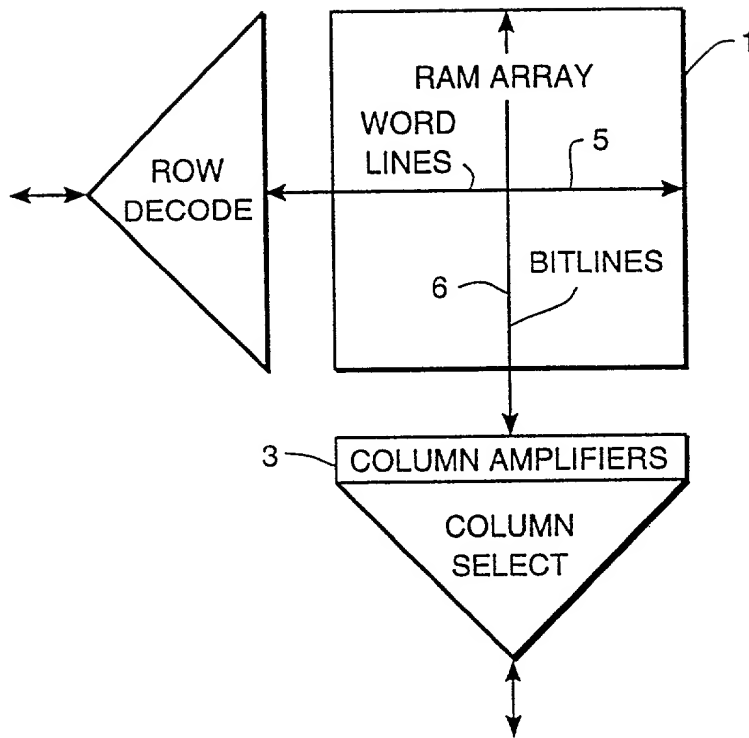
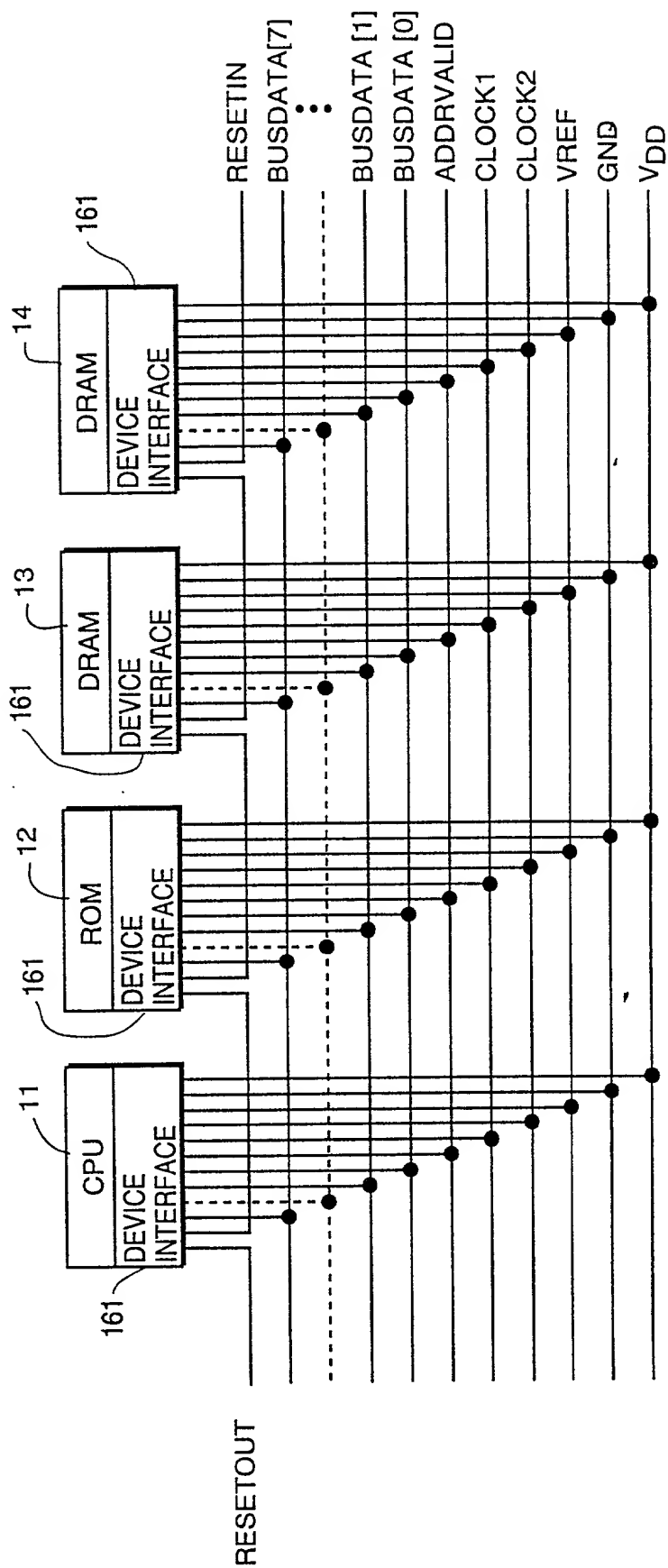
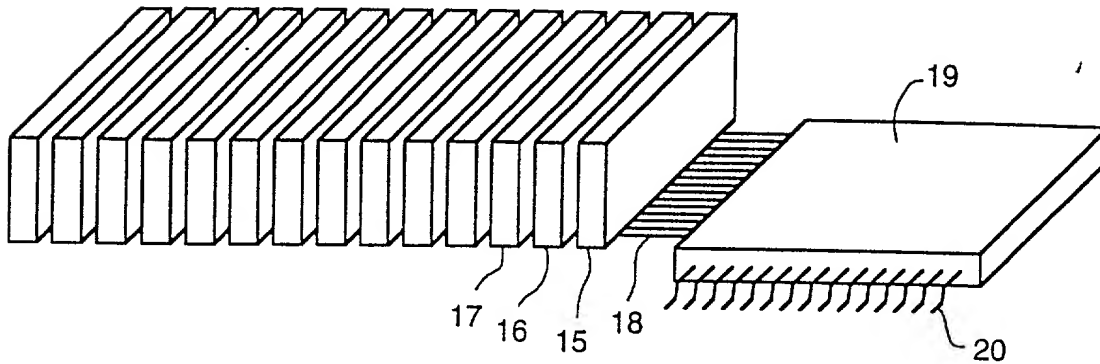


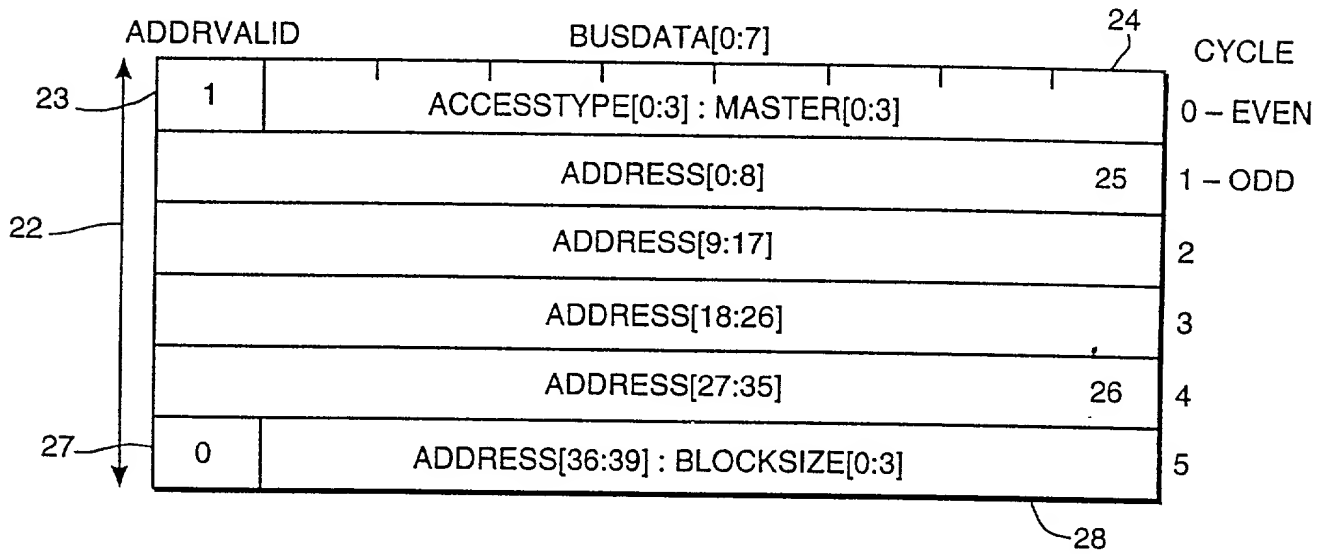
FIG. 2



**FIG 3**

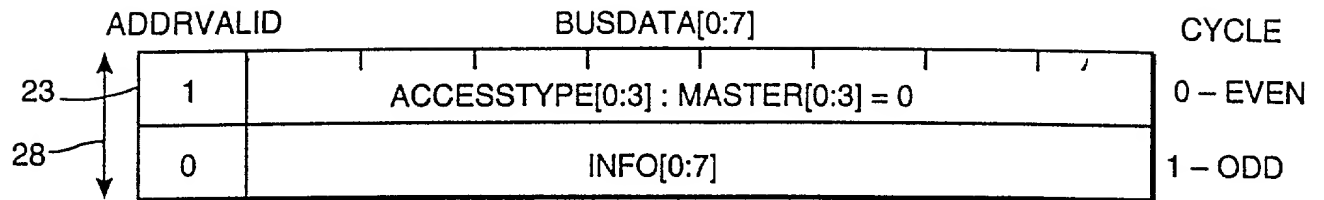


REGULAR ACCESS

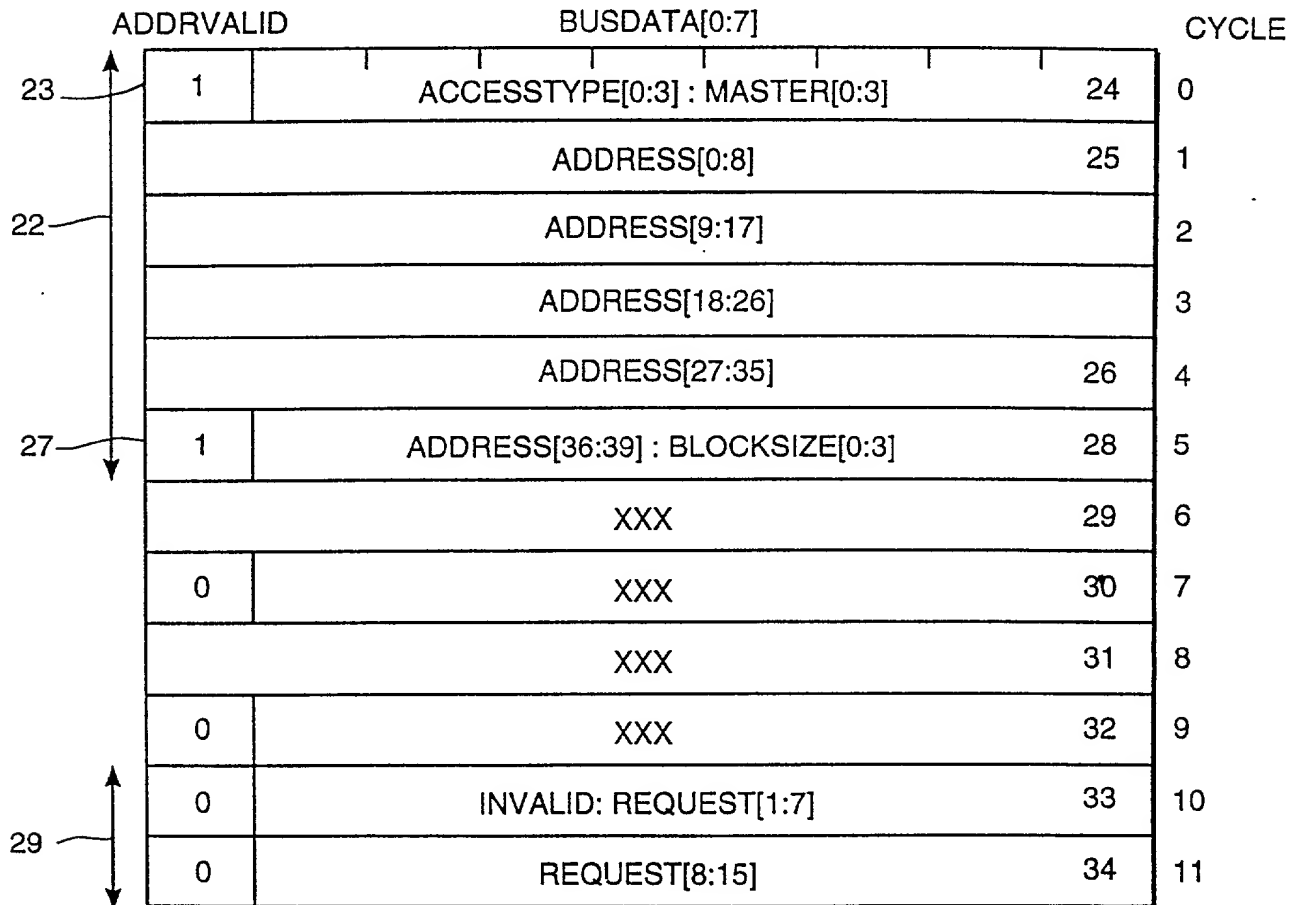


**FIG 4**

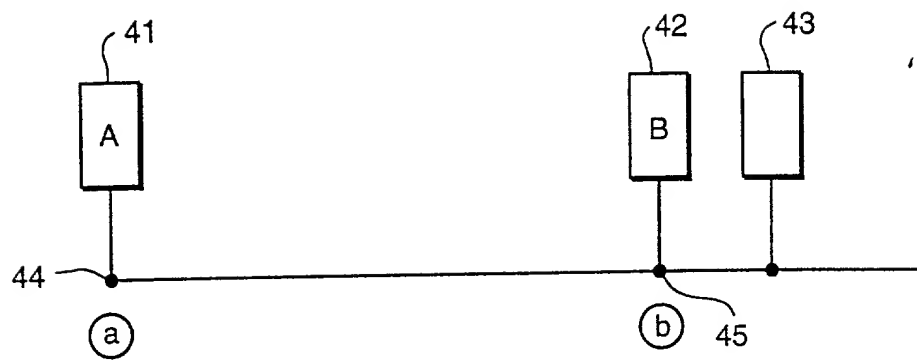
# REJECT (NACK) CONTROL PACKET



**FIG 5**



**FIG 6**



**FIG 7A**

FIG 7B

VOLTAGE LOGICAL  
VALUE

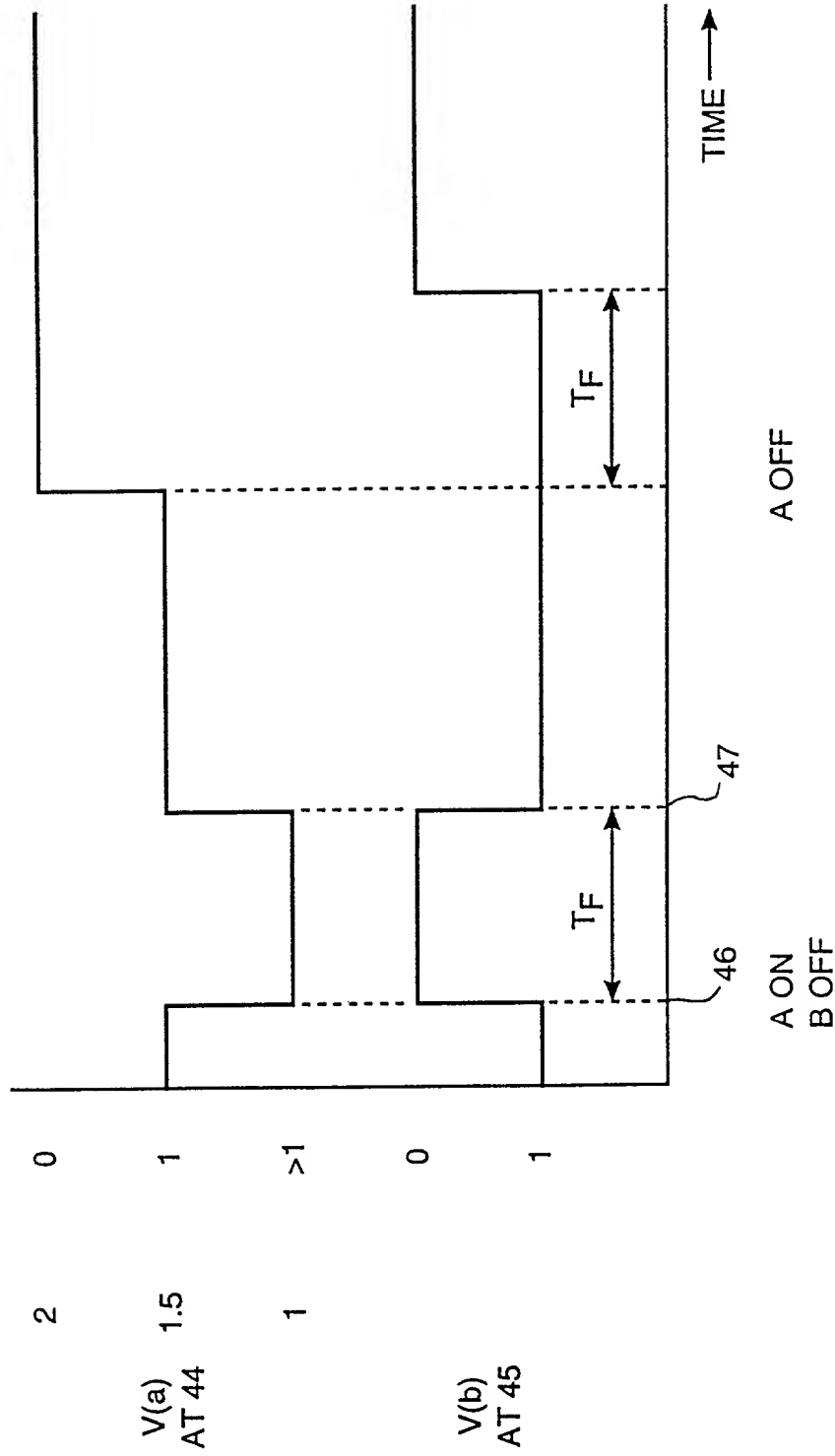
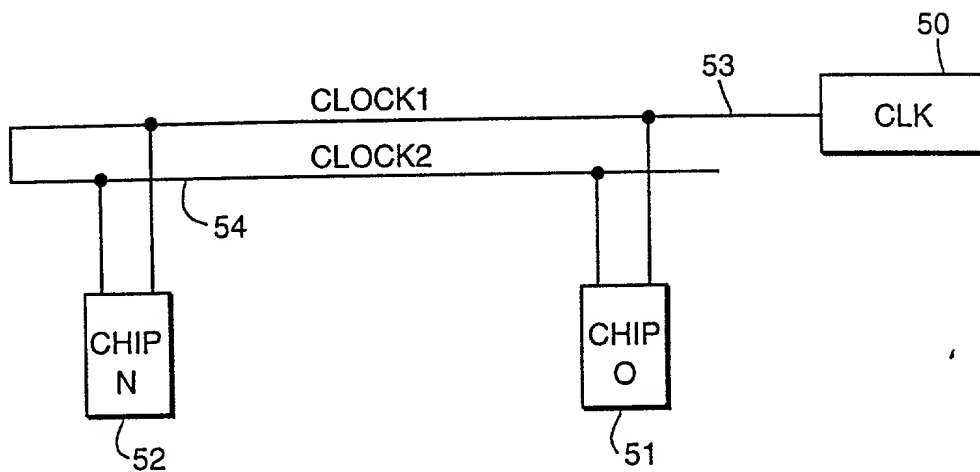
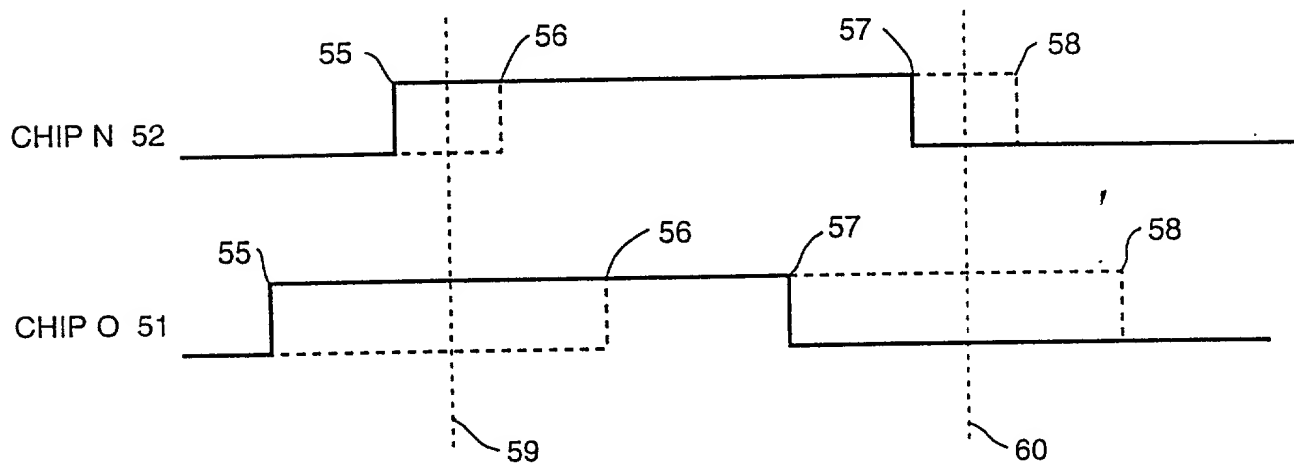


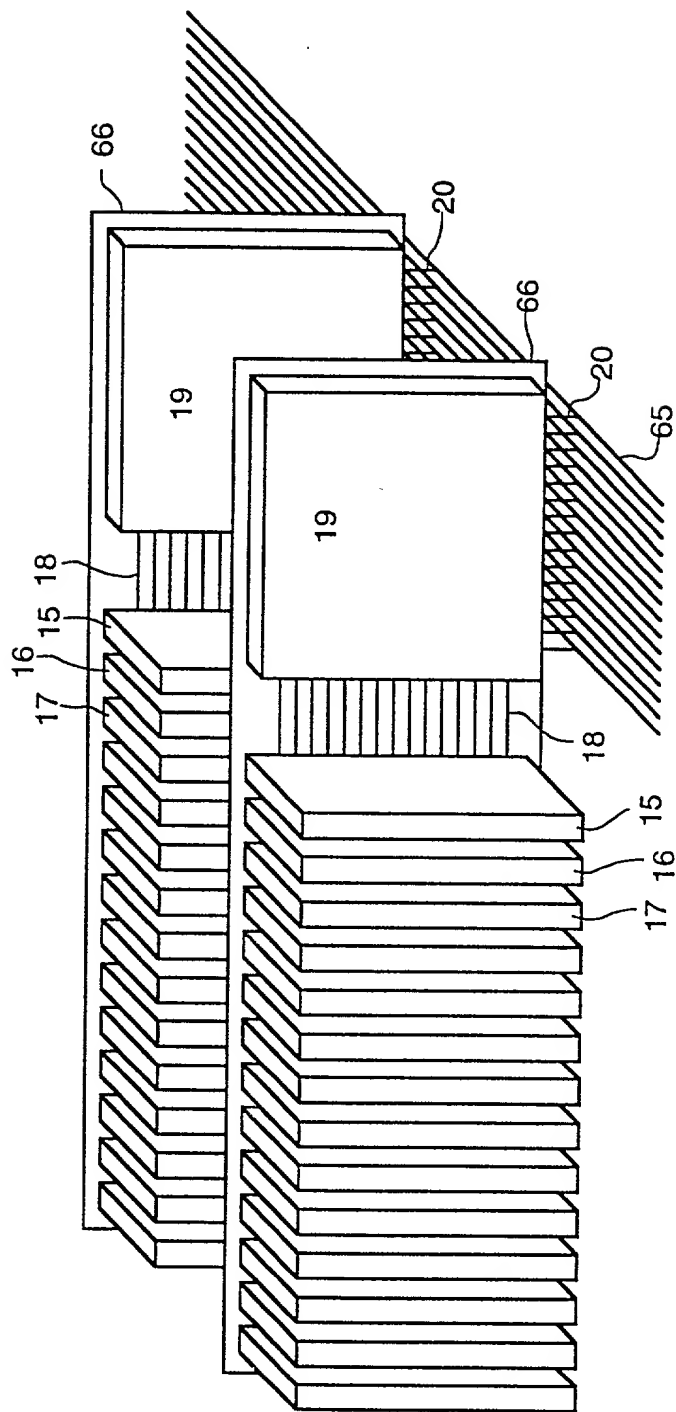
FIG 7B



**FIG 8A**



**FIG 8B**



**FIG. 9**

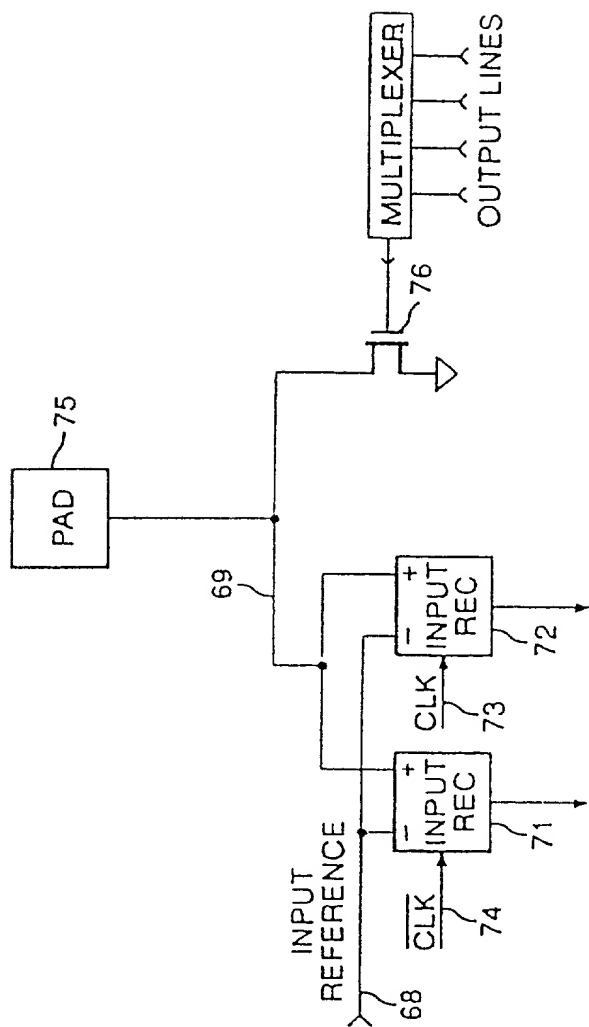
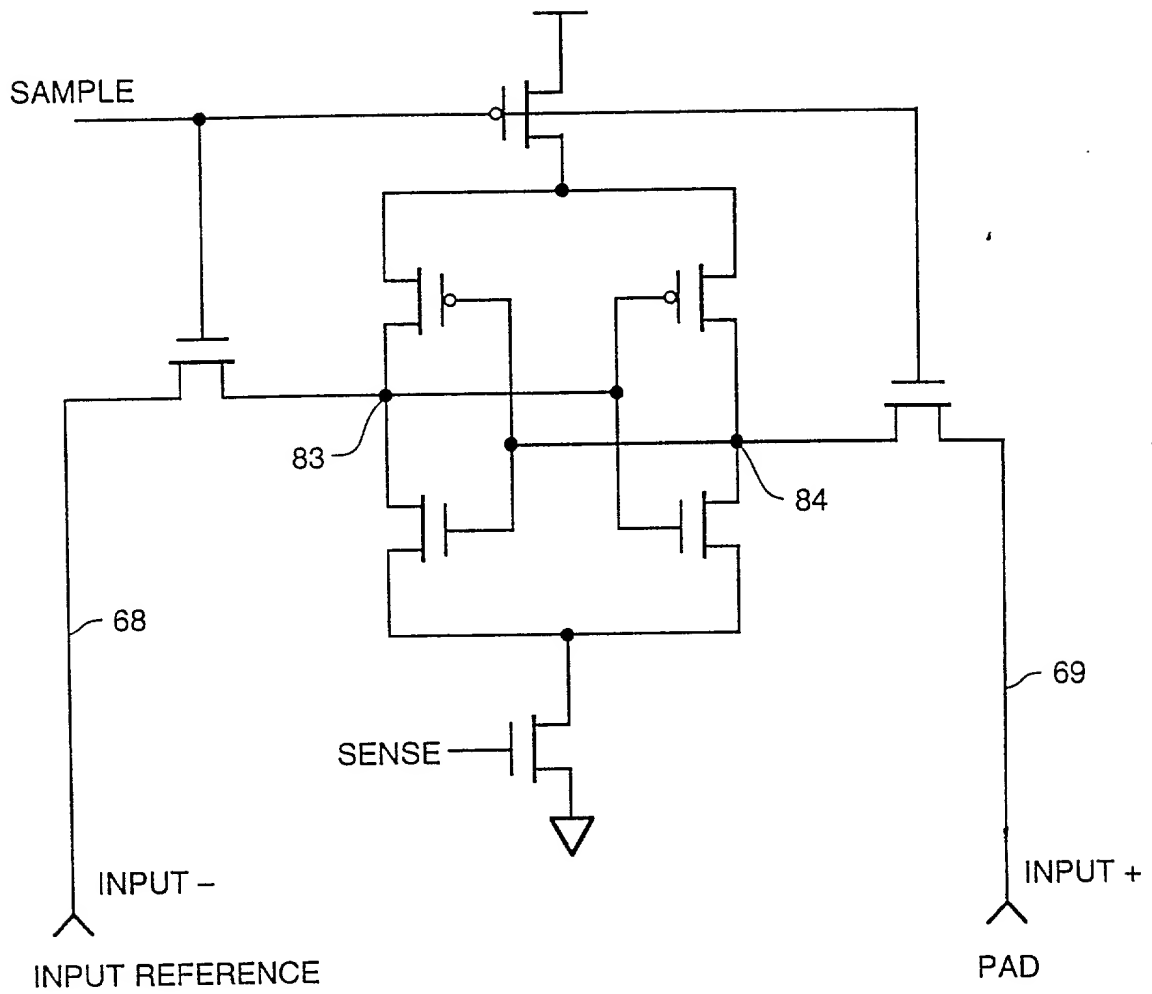
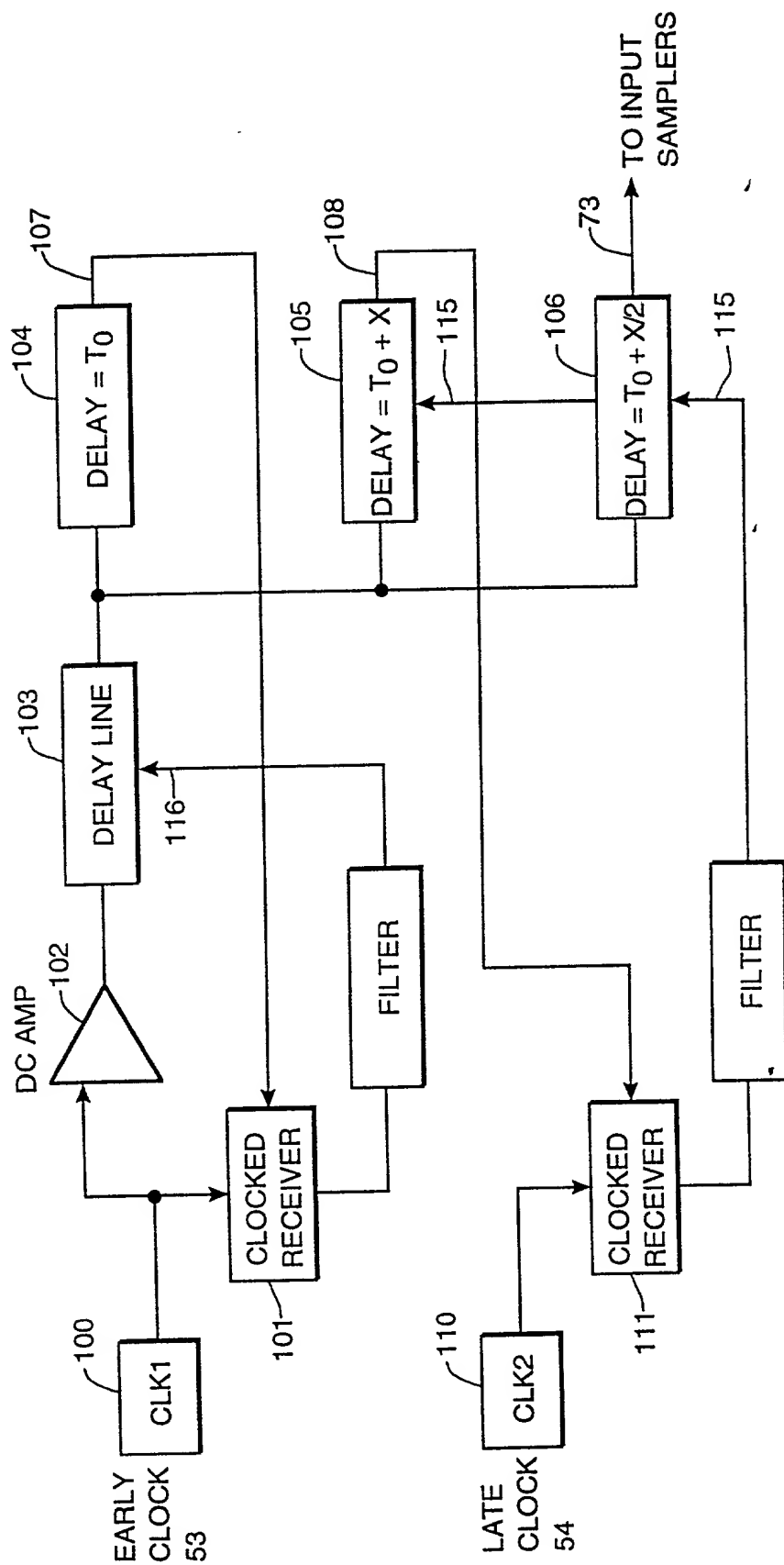


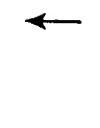
FIG. 10

**FIG. 11**



# FIG. 12





CLOCK



RESET IN



RESET OUT



BUS DATA [0:7]



**FIG 14**

**FIG 15**

